Advanced Packaging Lithography and Inspection Solutions for Next Generation FOWLP-FOPLP Processing

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Abstract

For more than 50 years the semiconductor industry has pursued Moore's law, continuously improving device performance, reducing cost, and scaling transistor geometries down to where advanced CMOS has reached beyond the 10nm technology node. The commensurate increase in I/O count has created many challenges for device packaging which hitherto was considered low cost with simple solutions. It was once thought that old backend foundry lithography steppers could be used to address the new packaging requirements; which was true whilst the substrates remained in the traditional 300mm Silicon format. The recent unprecedented rapid growth in Fan-out Wafer Level Packaging (FOWLP) applications has introduced a more complicated landscape of process challenges, with no restriction on substrate format, where cost is the main driver and high yields are mandatory.

This paper discusses the lithography process challenges that have ensued from disruptive FOWLP, and more recently the paradigm shift to Fan-out Panel Level Packaging (FOPLP). The work reports on lithography solutions for CD control over topography and high aspect ratio imaging of 2µm line/space RDL. In addition, the introduction of new inspection capabilities for defects and metrology is reported for both wafers and panels. The increase in lithography productivity and cost reduction provided by FOPLP is also discussed with production examples.

Key words

Fluorescence, FOWLP, Inspection, Panel, Stepper, Thick Resist

I. Introduction

With the ever increasing pressure to reduce costs and improve productivity, Out-Sourced Assembly and Test (OSAT) companies continuously make changes to their processing methods and substrate formats. In particular, moving from Silicon to reconstituted Epoxy Mold Compound (EMC) wafers has enabled the OSATs to become independent of substrate size & shape. Moreover, this freedom has enabled the use of large area panels which leverage economy of scale to further reduce costs, Fig. 1. shows the significant increase in die as a function of substrate size. Larger panel based substrates in back-end packaging processes promise significant reductions in cost per package. A 30-40% cost reduction of the panel can be achieved relative to round 300mm wafer fan-out. In addition to the economic benefit, panel fan-out packaging enables the industry to move to larger fan-out packages with multiple chip integration. However, panel scale fan-out processing presents a number of manufacturing and process control challenges. These includes chip placement on the carrier, molding, via reveal, Re-distribution layer (RDL) fabrication and final ball placement. OSATs are also continuously pushing for smaller line space pitch RDL on these fan-out packages. This drives the need for high resolution lithography and inspection systems that are capable of handling, patterning and inspecting large panels. In addition, BEOL processing induces stress to the substrates which results in significant warpage on both wafers and the panels, this presents additional challenges to not only handling but also detection of sub-micron defects.

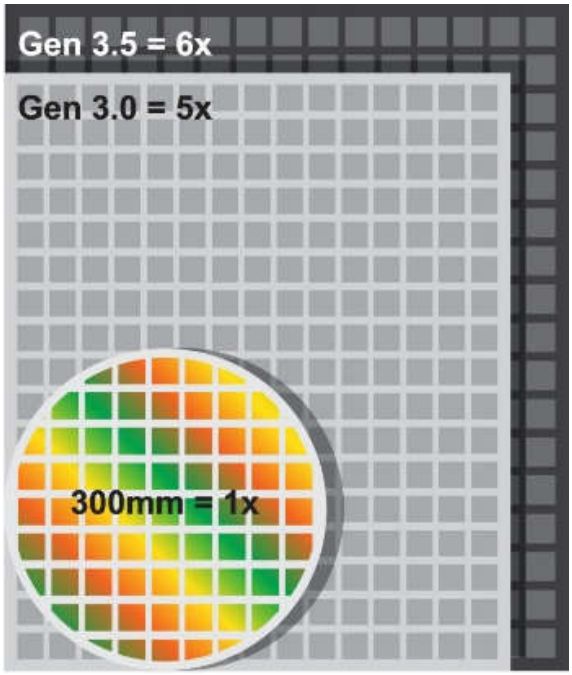

Fig. 1. Comparison of die exposed on 300mm Vs. Panel

II. Lithography Solutions

A. Lithography System Requirements

Fig. 2. JetStep® S3500 Panel Lithography System

Lithography remains a key requirement for advanced packaging of both wafers and panels. The JetStep S3500 Panel based lithography stepper Fig. 2 has a larger substrate exposure area than for wafers, the panel lithography system can also maintain an effectively larger exposure field size for every exposure as it is not constrained by the partial exposures associated with wafer edge processing. Exposing a larger field size per exposure reduces the number of exposures required per panel, resulting in higher throughput than wafers in terms of die per hour. Larger exposure field size also provides a means to avoid stitching of fields as fan-out die sizes become larger. To expose a larger field size and maintain overlay from layer to layer the lithography system also has the capability to correct for scale and magnification across the larger image field as well as compensate for die placement inaccuracy realized with reconstituted panels by the gantry used to populate the panel or curing of the EMC. A single telecentric lens system with adjustable reticle positioning for magnification, trapezoid in x and y, rotation, and xy translation is appropriate to achieve overlay with the larger exposure field. This capability enables corrections for intra field magnification, scale, theta and compliments corrections made by the xy stage for orthogonality, theta and scale.

B. Alignment and Overlay

Die placement on reconstituted panels used for fan-out are sensitive to the same constraints experienced with reconstituted wafers. Die placement accuracy by the gantry used for pick and place as well as the molding process contribute to die offsets on the substrates that must be understood by the lithography stepper to achieve targeted overlay. Another feature that is also beneficial, if utilized, is "mapping" of the panel to measure the actual die placement position in relation to its designed location and providing this information to the stepper for the best possible alignment solution to achieve overlay at different areas of the panel. Mapping of die location was first practiced in the 1980s on lithography steppers used in front-end applications. An example of a mapped panel is shown in Fig. 3.

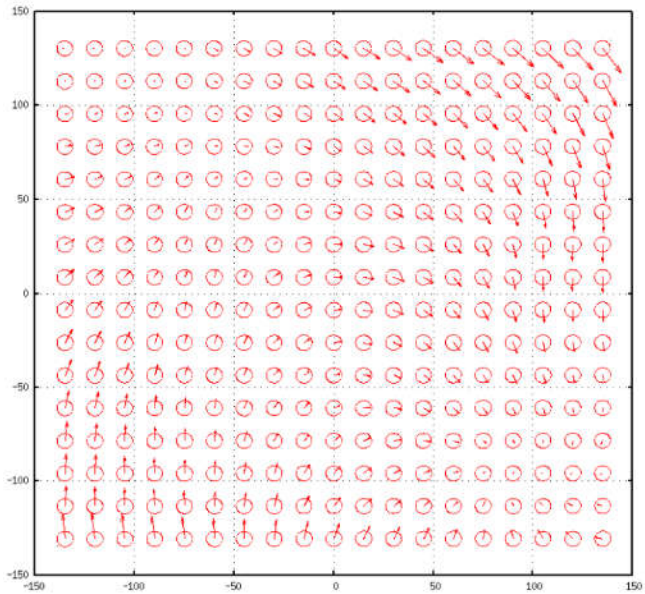

Fig. 3. Vector map of die placement offset on a reconstituted panel (Note: Circle radius = 4µm)

Numerous panels have been processed to investigate the adoption of panel-based advanced packaging. The panels were exposed on a Rudolph Technologies JetStep®

lithography system. The JetStep system is a 2x reduction lithography stepper with a single telecentric optical system that exposes a 59.4 x 59.4 mm exposure area on the panel while enabling magnification adjustment on a per panel basis along with grid corrections for scale. Magnification and scale can be corrected, up to ±400 ppm or 11.88 µm of correction from center to edge of exposure field (Fig. 4). Distortion is tightly controlled within <0.1µm of distortion over the magnification and scale adjustment range.

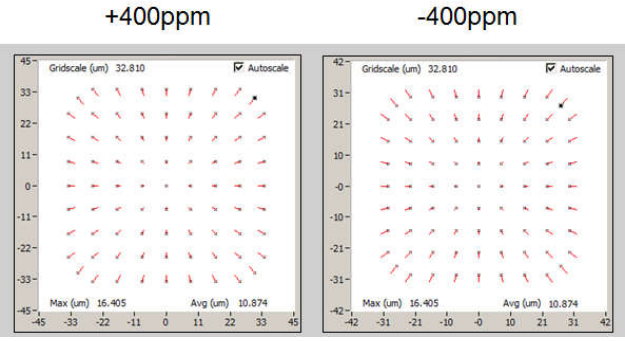

Fig. 4. Vector map showing available magnification and scale adjustment over an 84mm diameter lens field

C. Resolution and Depth of Focus

The paradigm shift in substrate dimensions, topography, and device architecture also result in imaging challenges, where 2µm line/space with large Depth Of Focus (DOF) in thick photoresist are prerequisites for success. Although resolution is not sub-micron, high aspect ratios can be expected and require optical systems with adequate numerical aperture (NA) to achieve desired resolution while imaging through the thick film and over the topography. Achievable resolution and DOF are determined by the following equations:

$$R = k_1\lambda/n.a. \quad (1)$$

$$DOF = k_2\lambda/NA^2 \quad (2)$$

Where k1 and k2 are process factors, λ is wavelength. Fig.5 shows SEM cross section of 2µm RDL in 10µm photoresist, DOF was measured to be >28µm with 0.1NA lens.

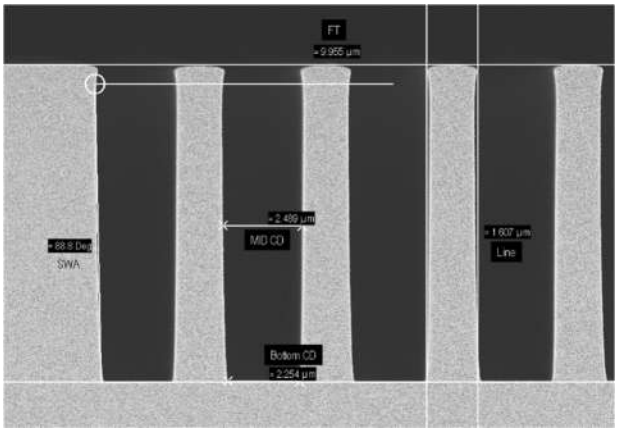

Fig. 5. 5:1 Aspect Ratio, 2µm RDL

D. Patterning Over Topography

Panels have larger area than wafers, they require focus to be set at every exposure location and for the lens to have enough DOF to accommodate topography. Fig. 6 shows 5µm RDL over a 6µm step where the resist thickness changes from 11µm to 17µm. This challenge typically occurs when reconstituted die, face up, are connected together.

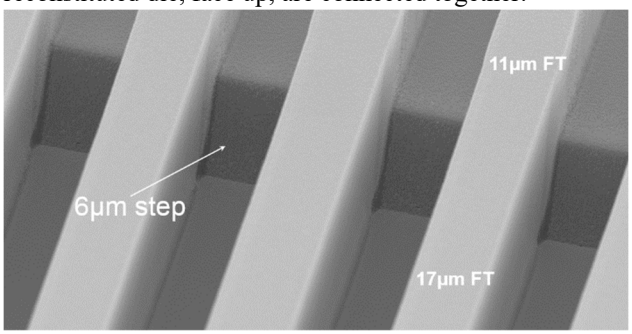

Fig. 6. Photoresist image of RDL over topography

E. Warpage

Warpage is recognized as an issue with 300 mm reconstituted wafers. The stepper and handling equipment must accommodate for warpage that is incurred due to the molding operation or various films that are deposited on the substrate. Panel warpage is also an area that will need to be addressed. Some of the handling characteristics currently employed in reconstituted wafer processing can be employed to handle panels, but panels also have unique characteristics that are different than wafers because they are rectangular in shape and flex and distort differently than a wafer. Steppers currently utilized for the manufacture of flat panels displays are experienced with handling large glass substrates of up to 920 mm x 730 mm at 0.3 mm thickness that flex considerably during handling. This technology along with can be utilized to successfully transfer and vacuum clamp panels used for advanced packaging to the stage chuck.

F. Panel Throughput Advantage

Manufacturing costs are a concern in any industry. For advanced packaging lithography the opportunity to move from circular wafers to rectangular substrates provides a means to reduce manufacturing costs by utilizing tool sets that have been developed for the production of flat panel displays, printed circuit boards and solar panels. All use manufacturing processes that can be applied to advanced packaging on large rectangular substrates.

Front-end lithography is performed on round wafers and die are lost at the edge of the wafer due to portions of the square die laying beyond the radius of the wafer. As discussed above, exposure fields for advanced packaging are large and can expose multiple die with each exposure. Since a wafer is populated to contain all known good die (KGD) within the exclusion area of the wafer the advantage of exposing multiple die in a large single exposure is compromised along the wafer edge because only a portion of the die are exposed, due to the way a wafer is populated, and the remaining exposure area is nonproductive because it lays in the wafer exclusion zone or off the edge of the wafer. It stands to reason that exposing a square or rectangular pattern fits more perfectly on a square or rectangular substrate and eliminates lost opportunity that occurs on wafers because a portion of the exposure area lies beyond the edge of a circular wafer Fig.7. Larger rectangular substrates also increase throughput by reducing nonproductive overhead required to exchange substrates.

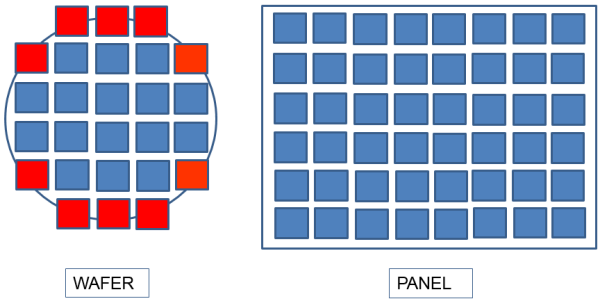

Fig. 7. Illustration of partial die exposure on a wafer compared to die exposure on a panel, non-productive areas of die on wafer shown in red

Productivity gains from exposing panels instead of wafers has been modeled by comparing exposure of various die sizes Table 1, Fig. 8. on a 600 x 600 mm² panel to the same die size on 300 mm diameter wafers. Processing conditions were 1500kW/cm² at ghi wavelength with nine alignment sites per substrate and substrate transfer constant at 14 seconds. Results show a productivity increase of >96% in the number of die realized per hour on the panel process over the wafer process.

Table I

	Panel		**Wafer**		
Die size mm²	*Die per 600 x 600mm² panel*	*Die per hour*	*Die per 300mm wafer*	*Die per hour*	*% Productivity increase per hour of panel over wafer*
4.05 x 2.6	28,350	643.5k	5,945	328k	96
2.44 x 2.44	51,750	1174 k	10,442	556k	111
4.95 x 5.4	10,800	246k	2,339	123k	100

Table II

Die size (mm²)	**Exposure Field at Substrate (mm²)**	**Exposures per Substrate**		**Substrates per Hour**	
		Wafer 300 mm	*Panel 600 x 600 mm²*	*Wafers*	*Panel*
4.05 x 2.6	61.87 x 56.200	25	100	55.3	21.7
2.44 x 2.44	62.885 x 57.848	27	100	53.3	20.9
4.95 x 5.4	60.28 x 54.720	28	90	52.5	22.8

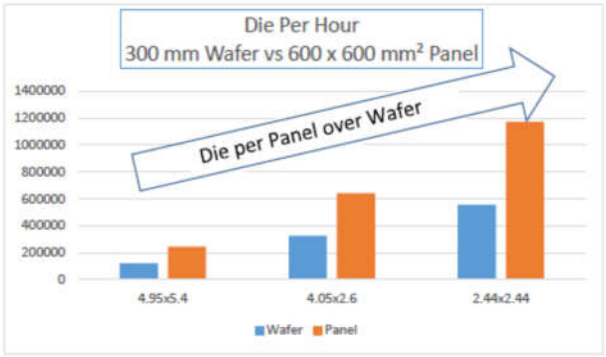

Fig. 8. Productivity increase that can be expected when processing on 600 x 600mm² panel over 300mm diameter wafer

The tables demonstrate the productivity advantage of exposing on rectangular substrates versus circular wafers. In panel processing, the number of exposures per panel increases due to the larger area of the panel and processed panels per hour are less then processed wafers per hour. However, the number of die populated on a panel is much greater than the

number of die populated on a wafer, resulting in a >89% productivity advantage when exposing on panels instead of wafers.

G. Inspection Solutions

To inspect warped wafer or panels for defects, Rudolph Technologies has developed Firefly™ Inspection system with ClearFind™ technology. ClearFind™ technology incorporates a dual focus system - a coarse z focus system that allows the optics to stay in the optimum focus range while a fine focus system which continuously measures the local topography as it scans the panel and adjusts focus automatically. This unique patented methodology allows the user to rapidly move the imaging objective and slowly move the optical head to maintain sharp imagery throughout the inspection. The system also has the ability to measure die placement error and compensate for die placement accuracy of each die independently in real time as it maintain focus while the panel is scanned. Die placement information along with inspection and metrology data are exported to yield management system for process learning and improving yield.

Firefly™ Inspection system is capable of detecting sub-micron defects using custom wide field optics along with the ability to use multiple illumination modes to address varying defect types. Multiple objectives allow the system to address packaging applications down to 2µm RDL L/S. Typically RDL defects of interest are half the size of the RDL width i.e. 1um for 2µm RDL. But in many cases, the acceptable metal graininess could be larger than the detection size. This leads to a high nuisance rate impacting the total throughput of the panel which includes manual review. ClearFind™ technology resolves this issue by incorporating a high speed sensor with dual focus system and fluorescent illumination. As the metal does not fluoresce and hence the metal grains are not detected as defects while finding 1µm open or short in the RDL lines. For cost effective deployment, the system is also integrated with a metrology sensor capable of simultaneous thickness measurement of transparent material and RDL height metrology. The inspection and metrology data is exported to Rudolph's Discover™ system to analyze electrical, metrology and defect data in a single source. This enables faster root cause analysis enabling quicker ramp and time to market.

Organic residue defects are not captured using traditional white light automated optical inspection (AOI) systems. Some manufacturers use a manual fluorescent microscope but it adds significant cost and introduces large variability in results. Firefly™ system with ClearFind™ technology provides a high-speed automated fluorescent inspection system that helps capture the organic residue reducing/eliminating defect escape. Fig.9.

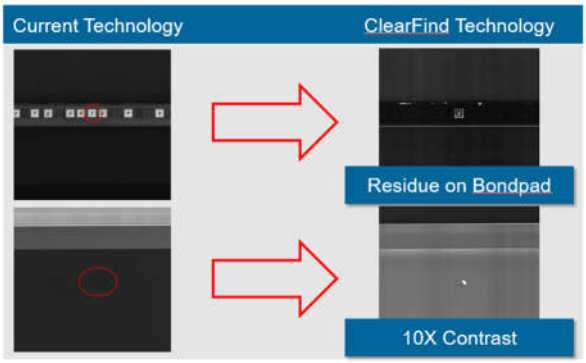

Fig. 9. Fluorescence solution: highlights organic resides on metal and array

III. Conclusion

Migrating from circular substrates to square or rectangular panels provides OSATS with the means to increase productivity per substrate processed. The improved fit between the mask and substrate on square or rectangular substrates, instead of circular wafers, during exposure eliminates nonproductive exposure of partial die about the periphery of a circular substrate and enables more die per substrate to be exposed. Exposing on panels provides a cost effective lithographic solution to an OSAT or foundry with a >89% productivity improvement over wafer-based processing.

The semiconductor industry has been a leader in adopting manufacturing technologies to fabricate devices with increased functionality while reducing manufacturing costs. This has enabled consumer acceptance and adoption of new technologies that are in demand throughout the world. Silicon wafers have increased in diameter from 4, 6, and 8 inches to 300 mm and eventually 450 mm. Implementing panel-based processing is not evolutionary, instead, it is the natural progression to achieve greater throughput at a cost advantage.

Acknowledgment

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